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Attorney's Docket No.: 42P15685

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Is/Re Patent Application of:

Scott A. Hareland et al.

Application No.: 10/607,769

Filed: June 27, 2002

For: NONPLANAR SEMICONDUCTOR  
DEVICE WITH PARTIALLY OR FULLY  
WRAPPED AROUND GATE ELECTRODE  
AND METHODS OF FABRICATION

Examiner: Unassigned

Art Unit: Unassigned

Commissioner for Patents  
P.O. Box 1450  
Alexandria, Virginia 22313-1450

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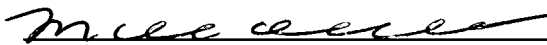
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Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 11/11, 2004

  
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## INFORMATION DISCLOSURE

## STATEMENT BY APPLICANT

(use as many sheets as necessary)

## Complete if Known

Application Number	10/607,769
Filing Date	June 27, 2003
First Named Inventor:	Scott A. Hareland
Art Unit	Unknown
Examiner Name	Unknown
Attorney Docket Number	42P15685

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## U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. <sup>1</sup>	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code <sup>2</sup> (If known)				
		US-	6,716,684 B1	4/6/2004	Krivokapic et al.	
		US-	6,680,240 B1	1/20/2004	Maszara	
		US-	6,562,665 B1	5/13/2003	Yu	
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		US-				
		US-				

## FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
		Country Code <sup>3</sup>	Number <sup>4</sup> Kind Code <sup>5</sup> (if known)				
			EP 0 623 963 A1	11/9/1994	Siemens AG		
			WO 02/43151A	5/30/2002	Hitachi ULSI Sys Co Ltd		

Examiner  
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Date Considered

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. <sup>1</sup>Applicant's unique citation designation number (optional). <sup>2</sup>See Kinds Codes of USPTO Patent Documents at [www.uspto.gov](http://www.uspto.gov) or MPEP 901.04. <sup>3</sup>Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>4</sup>For Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. <sup>5</sup>Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. <sup>6</sup>Applicant is to place a check mark here if English language translation is attached.

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**Complete if Known**

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**NON PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T <sup>2</sup>
		V. Subramanian et al., "A Bulk-Si-Compatible Ultrathin-body SOI Technology for Sub-100nm MOSFETS" Proceeding of the 57th Annual Device Research Conference, pp. 28-29 (1999)	
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		Huang et al., "Sub 50-nm FinFET: PMOS", 1999 IEEE International Electron Device Meeting Technical Digest, pp 67-70 (1999)	
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		Hisamoto et al., "A Fully Depleted Lean-Channel Transistor (DELTA)-A Novel Vertical Ultrathin SOI MOSFET", IEEE Electron Device Letters, V. 11(1), pp36-38 (1990).	
		Jong-Tae Park et al., "Pi-Gate SOI MOSFET" IEEE Electron Device Letters, Vol. 22, No. 8, August 2001, pages 405-406	
		Hisamoto, Digh et al. "FinFET- A Self-Aligned Double-Gate MOSFET Scalable to 20 nm", IEEE Transactions on Electron Devices, Vol. 47, No. 12, December 2000, pages 2320-2325	
		International Search Report PCT/US 03/26242	
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